EXHIBIT C

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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

ALPHA & OMEGA SEMICONDUCTOR, LTD., a Bermuda corporation; and ALPHA & OMEGA SEMICONDUCTOR, INC., a California corporation,

Plaintiffs and Counterdefendants,

v.

FAIRCHILD SEMICONDUCTOR CORP., a Delaware corporation,

Defendant and Counterclaimant.

AND RELATED COUNTERCLAIMS.

Case No. C 07-2638 JSW
(Consolidated with Case No. C-07-2664 JSW)

PLAINTIFFS' AND COUNTERDEFENDANTS' DISCLOSURE OF ASSERTED CLAIMS AND PRELIMINARY INFRINGEMENT CONTENTIONS PURSUANT TO PATENT L.R. 3-1

Plaintiffs and Counterdefendants Alpha & Omega Semiconductor, Ltd. and Alpha & Omega Semiconductor, Inc. (collectively, "AOS") hereby provide the following disclosures pursuant to Patent Local Rules 3-1 and 3-2.

As an initial matter, AOS notes that under the schedule set by the Court and the parties in this matter, AOS is providing this disclosure prior to receiving documents, interrogatory responses, or any other discovery from Fairchild Semiconductor Corp. ("Fairchild"). Accordingly, AOS reserves the right to supplement these disclosures as it obtains discovery from Fairchild or as otherwise permitted under the applicable rules.

I. Patent Local Rule 3-1 Disclosures

A. Identification of Infringed Claims of the Patents-In-Suit

In this litigation, AOS currently asserts that Defendant and Counterclaimant Fairchild Semiconductor Corp. ("Fairchild") infringes claim 7 of U.S. Patent No. 5,767,567 ("the '567 patent") and claims 1-6, 10, 11, 13, 15, 16, and 25-28 of U.S. Patent No. 5,907,776 ("the '776 patent").

B. Identification of Accused Instrumentalities

1. '567 Patent

Based on the information available to date, the Accused Instrumentalities that infringe the '567 patent include products and methods. Such products include without limitation each of the following Fairchild products, and all other Fairchild products employing a corresponding design: FDS6982S, FDS6675, FDS4435, and FDS8884 (collectively "Accused '567 Patent Products"). Such methods include without limitation the methods that are used to manufacture the Accused '567 Patent Products (collectively "Accused '567 Patent Methods"). AOS reserves the right to supplement and/or amend this identification after receiving discovery from Fairchild, and as permitted under the applicable rules.

2. '776 Patent

Based on the information available to date, the Accused Instrumentalities that infringe the '776 patent include without limitation the methods that are used to manufacture the following Fairchild products, and all other Fairchild products employing a corresponding design:

FDP047AN08A0, FDS4435BZ, FDP3652, and FDS6675BZ (collectively "Accused '776 Patent Products and "Accused '776 Patent Methods"). AOS reserves the right to supplement and/or amend this identification after receiving discovery from Fairchild, and as permitted under the applicable rules.

C. Claim Charts

Charts demonstrating the application of the asserted claims to the Accused Instrumentalities are attached as Exhibits A and B.

D. Identification of Type of Infringement

AOS believes that the Accused '567 Patent Products, Accused '776 Patent Products (collectively, "Accused Fairchild Products") and Accused '576 Patent Methods and Accused '776 Patent Methods (collectively, "Accused Fairchild Methods") identified in the preceding sections literally infringe claim 7 of the '567 patent and each of claims 1-6, 10, 11, 13, 15, 16, and 25-28 of the '776 patent. Even if a judge or jury were to conclude that an element of an asserted claim is not literally present in the Accused Products, or is not literally a step or combination of steps of the Accused Methods, AOS believes that the Accused Fairchild Products and Accused Fairchild Methods would still infringe each of those claims under the doctrine of equivalents because the Accused Fairchild Products and Accused Fairchild Methods would still include, at a minimum, an equivalent to each element of each asserted claim.

E. Identification of Priority Dates

AOS believes, at the present time, that none of the asserted claims of the '567 or '776 patents are entitled to claim priority to an earlier application.

F. AOS Products That Incorporate or Reflect the Claimed Inventions

See Exhibit C for a list of AOS products that practice the claimed inventions.

II. Patent Local Rule 3-2 Document Production

Concurrently with the service of this disclosure, AOS has produced documents pursuant to Patent L.R. 3-2.

Dated: August 31, 2007

MORGAN, LEWIS & BOCKIUS LLP

By: /s/ Daniel Johnson, Jr.
Daniel Johnson, Jr.
Attorneys for Plaintiffs and Counterdefendants ALPHA & OMEGA SEMICONDUCTOR, LTD. AND ALPHA & OMEGA SEMICONDUCTOR, INC.

CERTIFICATE OF SERVICE

I am employed in the City of Palo Alto, County of Santa Clara, State of California, I am over the age of 18 years and not a party to the within action. My business address is 2 Palo Alto Square, 3000 El Camino Real, Palo Alto, California 94306. On August 31, 2007, I caused copies of the attached document(s) described as follows:

PLAINTIFFS' AND COUNTERDEFENDANTS' DISCLOSURE OF ASSERTED CLAIMS AND PRELIMINARY INFRINGEMENT CONTENTIONS PURSUANT TO PATENT L.R. 3-1

to be served on:

Eric P. Jacobs, Esq.
TOWNSEND & TOWNSEND
2 Embarcadero Center, 8th Floor
San Francisco, CA 94111
Tel: 415.576.0200
Fax: 415.576.0300

_____(BY OVERNIGHT DELIVERY) I caused each such envelope to the addressee(s) noted above, with charges fully prepaid, to be sent by overnight delivery from Palo Alto, California. I am readily familiar with the practice of Morgan, Lewis & Bockius LLP for collection and processing of correspondence for overnight delivery, said practice being that in the ordinary course of business, mail is placed with the overnight delivery service on the same day as it is placed for collection.

__BY ELECTRONIC MAIL) The person whose name is noted below caused to be transmitted by electronic mail each such document to the addressee(s) noted above.

_X_(BY FIRST CLASS MAIL) I caused each such envelope to the addressee(s) noted above, with postage thereon fully prepaid, to be placed in the United States mail in Palo Alto, California. I am readily familiar with the practice of Morgan, Lewis & Bockius LLP for collection and processing of correspondence for mailing, said practice being that in the ordinary course of business mail is deposited in the United States Postal Service the same date as it is placed for collection; and

_____(BY FACSIMILE) The person whose name is noted below caused to be transmitted by facsimile each such document to the addressee(s) noted above; and

__(BY PERSONAL SERVICE) The person whose name is noted below caused to be delivered by hand each such envelope to the addressee(s) noted above.

I declare under penalty of perjury under the laws of the State of California that the foregoing is true and correct. Executed at Palo Alto, California, on August 31, 2007.

/s/
Ahren Hoffman

EXHIBIT A - U.S. Patent No. 5,907,776

Claim 1	Accused '776 Patent Methods
1. A method of forming a semiconductor structure comprising the steps of:	AOS does not express a position at this time as to whether the preamble of this claim limits the claim's scope. Nevertheless, AOS identifies here those aspects of the Accused '776 Patent Methods that correspond to the preamble. The Accused '776 Patent Methods are methods of forming a semiconductor structure.
(a) providing a substrate having a major surface;	The Accused '776 Patent Methods include the step of forming a substrate. The resulting substrate has a top surface.
(b) forming at least one trench in said substrate;	The Accused '776 Patent Methods include the step of forming at least one trench gate in the aforementioned substrate.
(c) forming a body region of a first conductivity type in said substrate,	The Accused '776 Patent Methods include the step of forming a body region in the aforementioned substrate. The resulting body region is of a particular conductivity type.
said body region having a diffusion boundary in said substrate;	The resulting body region also has a diffusion boundary in the aforementioned substrate.
(d) forming a source region of a second conductivity type in said body region; and	The Accused '776 Patent Methods include the step of forming a source region in the aforementioned body region. The resulting source region is of a different conductivity type from the body region.
(e) compensating a portion of said body region by implanting material of said second conductivity type in said body region,	The Accused '776 Patent Methods include the step of compensating a portion of the aforementioned body region. This step includes at least implanting dopants of the same conductivity type as the aforementioned source region.
said portion being proximal to said source region and spaced from said diffusion boundary of said body region and said major so as to reduce the impurity concentration of said first conductivity type in said portion of said body region.	The compensated portion of the body region is near the source region but away from the aforementioned diffusion boundary and the aforementioned top surface of the substrate.

Claim 2	Accused '776 Patent Methods
2. The method of forming a semiconductor structure as set forth in claim 1 further including filling said at least one trench with N-type material.	Those of the Accused '776 Patent Methods used to manufacture Fairchild's N-channel products include the step of filling at least one trench with N-type material.

Claim 3	Accused '776 Patent Methods
3. The method of forming a semiconductor structure set forth in claim 1 wherein step (a) includes providing a base substrate of said second conductivity type and forming an epitaxial layer of said second conductivity type above said base substrate.	In the Accused '776 Patent Methods, the aforementioned step of forming a substrate includes the steps of (1) providing a base substrate of the same conductivity type as the aforementioned source region and (2) forming an epitaxial layer of the same conductivity type as the source region above the base substrate.

Claim 4	Accused '776 Patent Methods
4. The method of forming a semiconductor structure as set forth in claim 1 wherein step (c) includes the substeps of ion implanting material of said body region in said substrate and thereafter diffusing said material of said body region in said substrate.	In the Accused '776 Patent Methods, the aforementioned step of forming a body region includes the steps of ion implanting dopants and subsequently diffusing the dopants in the aforementioned substrate.

Claim 5	Accused '776 Patent Methods
5. The method of forming a semiconductor structure as set forth in claim 1 wherein step (d) includes the substeps of ion implanting material of said source region in said substrate and thereafter diffusing said material of said source region in said body region.	In the Accused '776 Patent Methods, the aforementioned step of forming a source region includes the steps of ion implanting dopants and subsequently diffusing the dopants in the aforementioned body region.

Claim 6	Accused '776 Patent Methods
6. The method of forming a semiconductor structure as set forth in claim 5 wherein step (e) includes ion implanting material of said second conductivity type in said body region at a predetermined distance from said source region.	In the Accused '776 Patent Methods, the aforementioned step of compensating a portion of the body region includes the step of ion implanting dopants of the same conductivity type as the aforementioned source region at a distance away from the source region.

Claim 10	Accused '776 Patent Methods
10. The method of forming a semiconductor structure as set forth in claim 1 further comprising forming a gate region formed of material of N-type conductivity dielectrically separated from said body region.	Those of the Accused '776 Patent Methods used to manufacture Fairchild's N-channel products further include the step of forming a gate region of N-type material. The resulting gate region is dielectrically separated from the aforementioned body region.

Claim 11	Accused '776 Patent Methods
11. The method of forming a semiconductor structure as set forth in claim 1 wherein said first conductivity type is of N-type and said second conductivity is of P-type.	In the Accused '776 Patent Methods used to manufacture Fairchild's N-channel products, the first conductivity type, which is the conductivity type of the resulting body region, is of N-type conductivity; the second conductivity type, which is the conductivity type of the resulting source region, is of P-type conductivity.

Claim 13	Accused '776 Patent Methods
13. A method of forming a semiconductor structure having a trench gate with a gate threshold voltage, said method comprising the steps of:	AOS does not express a position at this time as to whether the preamble of this claim limits the claim's scope. Nevertheless, AOS identifies here those aspects of the Accused '776 Patent Methods that correspond to the preamble. The Accused '776 Patent Methods are methods of forming a semiconductor structure.
(a) providing a substrate having a major surface;	The Accused '776 Patent Methods include the step of forming a substrate. The resulting substrate has a top surface.
(b) forming a body region of a first conductivity type in said substrate,	The Accused '776 Patent Methods include the step of forming a body region in the aforementioned substrate. The resulting body region is of a particular conductivity type.
said body region having a diffusion boundary in said substrate;	The resulting body region also has a diffusion boundary in the aforementioned substrate.
(c) forming a source region of a second conductivity type in said body region; and	The Accused '776 Patent Methods include the step of forming a source region in the aforementioned body region. The resulting source region is of a different conductivity type from the body region.
(d) compensating a portion of said body region by implanting material of said second conductivity type in said body region	The Accused '776 Patent Methods include the step of compensating a portion of the aforementioned body region. This step includes at least implanting dopants of the same conductivity type as the aforementioned source region.
adjacent to said source region and spaced from said diffusion boundary of said body region and	The compensated portion of the body region is near the source region but away from the aforementioned diffusion boundary and the aforementioned top surface of the substrate.

said major surface such that the impurity concentration of said portion of said body region is substantially reduced so as to decrease the gate threshold voltage of said trench gate.	

Claim 15	Accused '776 Patent Methods
15. The method of forming a semiconductor structure as set forth in claim 13 wherein step (d) includes ion implanting material of said second conductivity type in said body region at a predetermined distance from said source region.	In the Accused '776 Patent Methods, the aforementioned step of compensating a portion of the body region includes the step of ion implanting dopants of the same conductivity type as the aforementioned source region at a distance away from the source region.

Claim 16	Accused '776 Patent Methods
16. The method for forming a semiconductor structure as set forth in claim 15 wherein step (d) further including diffusing said compensated portion of said body region in said body region.	In the Accused '776 Patent Methods, the aforementioned step of compensating a portion of the body region includes the step of diffusing the compensated portion of the body region.

Claim 25	Accused '776 Patent Methods
25. A method of forming a semiconductor structure having a gate with a gate threshold voltage, said method comprising the steps of:	AOS does not express a position at this time as to whether the preamble of this claim limits the claim's scope. Nevertheless, AOS identifies here those aspects of the Accused '776 Patent Methods that correspond to the preamble. The Accused '776 Patent Methods are methods of forming a semiconductor structure.
(a) providing a substrate having a major surface;	The Accused '776 Patent Methods include the step of forming a substrate. The resulting substrate has a top surface.
(b) forming at least one trench in said substrate extending from said major surface;	The Accused '776 Patent Methods include the step of forming at least one trench in the aforementioned substrate. The resulting trench extends from the top surface of the aforementioned substrate.
(c) forming a body region of a first conductivity type in said substrate	The Accused '776 Patent Methods include the step of forming a body region in the aforementioned substrate. The resulting body region is of a particular conductivity type.
to a diffusion boundary extending from said major surface;	The resulting body region also has a diffusion boundary to which it extends in the substrate from the aforementioned top surface of the substrate.
(d) forming a source region of a	The Accused '776 Patent Methods include the step of forming a

second conductivity type in said body layer extending from said major surface; and	source region in the aforementioned body region. The resulting source region is of a different conductivity type from the body region. The resulting source region also extends from the aforementioned top surface of the substrate.
(e) compensating a portion of said body region by implanting material of said second conductivity type in said body region	The Accused '776 Patent Methods include the step of compensating a portion of the aforementioned body region. This step includes at least implanting dopants of the same conductivity type as the aforementioned source region.
adjacent to said source region and spaced from said diffusion boundary of said body layer and said major surface such that the conductivity of said portion of said body region is substantially reduced so as to decrease the gate threshold voltage of said gate.	The compensated portion of the body region is near the source region but away from the aforementioned diffusion boundary and the aforementioned top surface of the substrate.

Claim 26	Accused '776 Patent Methods
26. The method of forming a semiconductor structure as set forth in claim 25 wherein step (b) includes the substep of lining said trenches with insulating material and followed by another substep of filing said trenches with conductive material.	In the Accused '776 Patent Methods, the aforementioned step of forming at least one trench includes the steps of lining the at least one trench with insulating material and subsequently filling the at least one trench with conductive material.

Claim 27	Accused '776 Patent Methods
27. The method of forming a semiconductor structure as set forth in claim 26 wherein said conductive material is a N-type material.	In the Accused '776 Patent Methods used to manufacture Fairchild's N-channel products, the aforementioned conductive material with which the at least one trench is filled is an N-type material.

Claim 28	Accused '776 Patent Methods
28. The method of forming a semiconductor structure as set forth in claim 25 wherein step (e) includes ion implanting material of said second conductivity type in said body region at a predetermined distance from said source region.	In the Accused '776 Patent Methods, the aforementioned step of compensating a portion of the body region includes the step of ion implanting dopants of the same conductivity type as the aforementioned source region at a distance away from the source region.

EXHIBIT B - U.S. Patent No. 5,767,567

Claim 7	Accused '567 Patent Methods
7. A method to configure a source contact area on a power MOSFET device by dividing said source contact areas with several gate runners disposed thereon, said method including steps of:	AOS does not express a position at this time as to whether the preamble of this claim limits the claim's scope. Nevertheless, AOS identifies here those aspects of the Accused '567 Patent Methods that correspond to the preamble. The Accused '567 Patent Methods are used to configure at least one source contact area on a power MOSFET integrated circuit ("IC") device. The Accused '567 Patent Methods include dividing the at least one source contact area with one or more gate runners.
(a) determining a total number of lead wires for connecting to a lead frame from said source contact area on said MOSFET power device; and	The Accused '567 Patent Methods include the step of determining a total number of lead wires for connecting to the at least one lead frame from a given source contact area.
(b) configuring said gate runners for dividing said source contact area into several sub-contact areas with a set of area proportional ratios for disposing several of said lead wires in each of said sub-contact areas according to said set of area proportional ratios.	The Accused '567 Patent Methods include the step of dividing the source contact area with the one or more gate runners into two or more subsections. The subsections of the source contact area are divided so that they are of proportional ratios for disposing the lead wires in accordance with the ratios.

EXHIBIT C

AOS Products Practicing the Claimed Inventions (by Part Number)

AO4407
AO4407
AO4407L
AO4409
AO4409-BD
AO4409L
AO4410-BD
AO4410-BD
AO4411-BD
AO4411-BD
AO4411-BD
AO4411L-BD
AO4413-BD
AO4413-BD
AO4413L-BD
AO4413L-BD
AO4415-BD
AO4415-BD
AO4415-BD
AO4415L-BD
AO4417-BD
AO4417-BD
AO4417-BD
AO4418A_100-BD
AO4418-BD
AO4418-BD
AO4418-BD
AO4418L-BD
AO4421-BD
AO4421L-BD
AO4422A-BD
AO4422A-BD
AO4422A-BD
AO4422AL
AO4422-BD
AO4422-BD
AO4422-BD
AO4422-BD
AO4422L-BD
AO4423-BD
AO4423L-BD
AO4428-BD
AO4428-BD
AO4429-BD
AO4429-BD
AO4429L-BD
AO4430
AO4430A_100-BD
AO4430-BD
AO4430-BD
AO4430-BD
AO4430-BD
AO4430L-BD
AO4431-BD
AO4431-BD
AO4431-BD
AO4436-BD
AO4438-BD
AO4438-BD
AO4438L-BD
AO4439-BD
AO4439-BD
AO4439-BD
AO4439L-BD
AO4446-BD
AO4446-BD
AO4446-BD
AO4447-BD
AO4449_100-BD
AO4449-BD
AO44451_100-BD
AO44451-BD
AO4556_100-BD
AO4456-BD
AO4462_100-BD
AO4462-BD
AO4468-BD
AO4468_100-BD
AO4468-BD
AO4470_100-BD
AO4470-BD
AO4472_100-BD
AO4472-BD
AO4474_100-BD
AO4474-BD
AO4476_100-BD
AO4476-BD
AO4702-BD
AO4702-BD
AO4702L-BD
AO4703-BD
AO4705-BD
AO4706_100-BD
AO4706-BD
AO4707-BD
AO4708_100-BD
AO4708-BD
AO4709-BD
AO4709-BD
AO4709-BD
AO4716_100-BD
AO4716-BD
AO4718_100-BD
AO4718-BD
AO4726_100-BD
AO4818B_100-BD
AO4818B-BD
AO4818-BD
AO4818-BD
AO4818L-BD
AO4822_100-BD
AO4822A-BD
AO4822A-BD
AO4822AL-BD
AO4822-BD
AO4822L-BD
AO4824L-BD
AO4912-BD
AO4912L-BD
AO4916A-BD
AO4916-BD
AO4916L-BD
AO4918A-BD
AO4918AL-BD
AO4918-BD
AO4918L-BD
AO4930_100-BD
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AO4932_100-BD
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AO4938_100-BD
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AOD402-BD
AOD402L-BD
AOU405L-BD